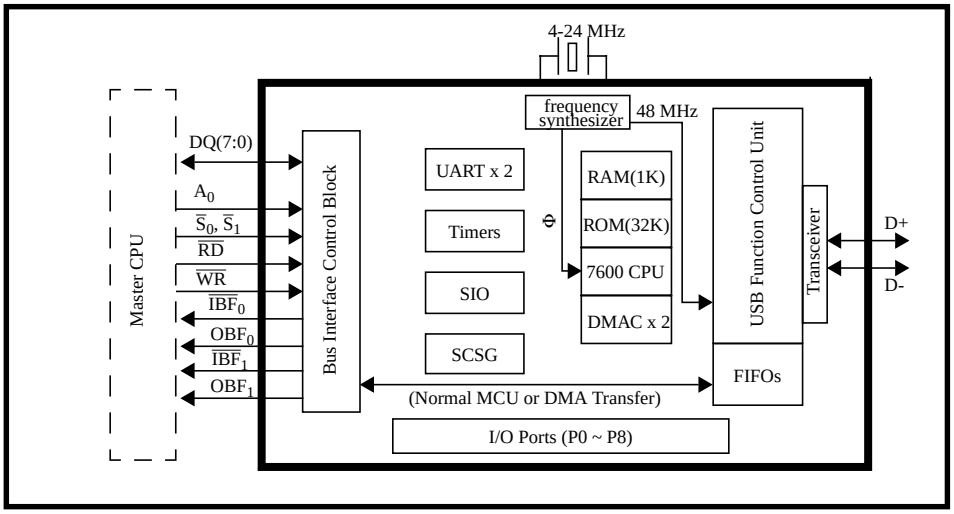
M37641M8

OVERVIEW:

- **Compatibility with M37640E8/M8.**
- **Added 3.3v only enviroment option.**
- **Expanded USB FIFO sizes for full bandwidth isochronous applications.**
- **Additional LQFP package option.**

APPLICATION SYSTEM DIAGRAM:



FEATURES:

Parameter			Function Description
Number of basic instructions			71 instructions, 7600 8-bit CPU core, backwards compatible with M37640E8/M8
Instruction execution time (minimum)			83ns at Φ = 12 MHz
Clock frequency (maximum)			**Xin = 48 MHz, XC_{in} = 5 MHz (square wave), Φ = 12 MHz, Vcc = 4.15 ~ 5.25V** **Xin = 48 MHz, XC_{in} = 5 MHz (square wave), Φ = 6MHz, Vcc = 3.00 ~ 3.6V**
Clock multiplier option			External clock X_{in} and XC_{in} can be selectively divided and multiplied by X to create system internal clock Φ
Memory size	ROM		32K bytes
	RAM		1K bytes
Input/Output ports	P0~P3, P5, P6, P8	I/O	8-bit X 7 (Port 2 has a key-on wake-up feature)
	P4, P7	I/O	5-bit X 2
USB Function Control			FIFO: Endpoint 0: IN 16-byte OUT 16-byte Endpoint 1: **Mode 00:** IN 512-byte OUT 800-byte **Configurable via Mode Register 5F** **Mode 01: IN 1K-byte OUT 1K-byte** **Mode 10: IN 0 -byte OUT 2K-byte** **Mode 11: IN 2K-byte OUT 0-byte** Endpoint 2: IN 32-byte OUT 32-byte Endpoint 3: IN 16-byte OUT 16-byte Endpoint 4: IN 16-byte OUT 16-byte
USB Transceiver			**Conforms to USB Specification V1.1, Electrical Characteristics for self-powered and bus-powered applications.**
Master CPU bus interface			DQ(7:0), $\overline{R}$(E), $\overline{W}$(R/$\overline{W}$), $\overline{S}_0$, $\overline{S}_1$, A_0, $\overline{IBF}_0$, OBF_0, $\overline{IBF}_1$, OBF_1; total of 17 signals interface with master CPU (Intel 8042-like interface)

Parameter	Function Description
Special Count Source Generator(SCSG)	Baud rate synthesizer
UART X 2	7/8/9-bit character length, with $\overline{CTS}$, $\overline{RTS}$ available
Serial I/O	8-bit clock synchronous serial I/O, supports both master and slave modes
Timers	8-bit X 3, 16-bit X 2
DMAC	2 channels, 16 address lines, support single byte or burst transfer modes
Software selectable slew rate control	Ports P0 ~ P8
Interrupts	4 external, 19 internal, 1 software, 1 system interrupts
Supply voltage	**V_{cc} = 4.15 ~ 5.25V or 3.0 ~ 3.6 V**
Power saving	**IDLE and STOP Modes**
External memory expansion	Memory Expansion and Microprocessor mode
External Data Memory Access (EDMA)	Allows > 64 Kbyte data access for instruction LDA (indY) and STA (indY)
Device structure	CMOS
Package	80P6N, 80P6Q
Operating temperature range	-20 to 85^{o}C

PIN LAYOUT:

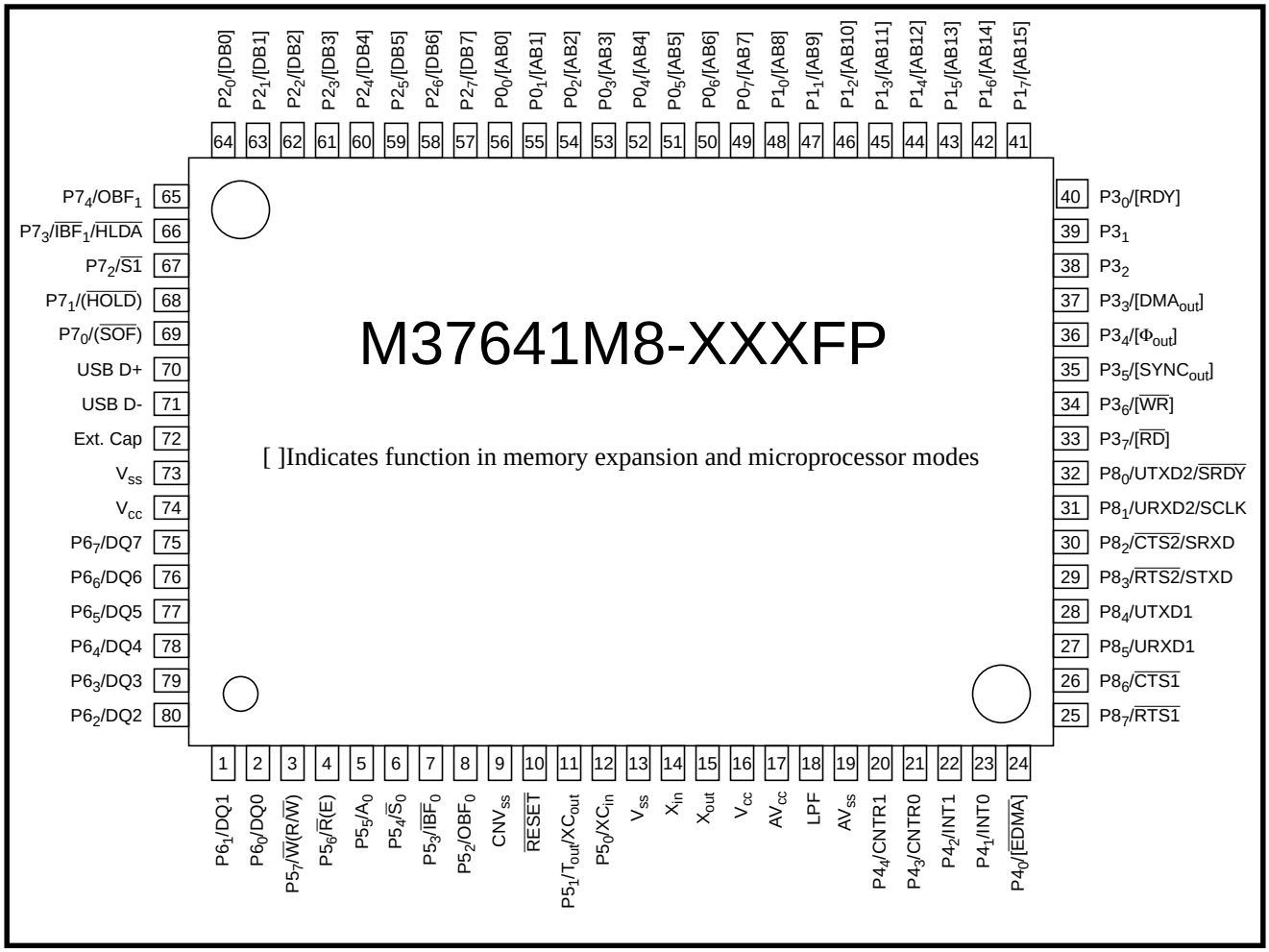


Figure 0-1. Pin Layout

PIN DESCRIPTION:

Name	I/O	Description	Pin #
$P0_0$/AB0 ~ $P1_7$/AB15	I/O	CMOS I/O port (address bus). When the MCU is in memory expansion or microprocessor mode, these pins function as the address bus.	56-41
$P2_0$/DB0 ~ $P2_7$/DB7	I/O	CMOS I/O port (data bus). When the MCU is in memory expansion or microprocessor mode, these pins function as the data bus. These pins may also be used to implement the Key-on Wake up function.	64-57
$P3_0$/RDY	I/O	CMOS I/O port (Ready). When the MCU is in memory expansion or microprocessor mode, this pin functions as RDY (hardware wait cycle control).	40
$P3_1$	I/O	CMOS I/O port.	39
$P3_2$/(VRFY)	I/O	CMOS I/O port. When the MCU is in EPROM program mode, the pin is used as VRFY (EPROM memory verify).	38
$P3_3$/DMA_{out} /$\overline{PGM}$	I/O	CMOS I/O port (DMA_{out}). When the MCU is in memory expansion or microprocessor mode, this pin is set to a "1" during a DMA transfer. When the MCU is in EPROM program mode, the pin is used as $\overline{PGM}$ (EPROM memory program).	37
$P3_4$/Φ_{out}	I/O	CMOS I/O port (Φ). When the MCU is in memory expansion or microprocessor mode, this pin becomes Φ_{out} pin.	36
$P3_5$/$SYNC_{out}$	I/O	CMOS I/O port (SYNC output). When the MCU is in memory expansion or microprocessor mode, this pin becomes the SYNCout pin.	35
$P3_6$/$\overline{WR}$/($\overline{CE}$)	I/O	CMOS I/O port. ($\overline{WR}$ output). When the MCU is in memory expansion or microprocessor mode, this pin becomes $\overline{WR}$. When the MCU is in EPROM program mode, the pin is used as $\overline{CE}$ (EPROM memory chip enable).	34
$P3_7$/$\overline{RD}$/($\overline{OE}$)	I/O	CMOS I/O port. ($\overline{RD}$ output). When the MCU is in memory expansion or microprocessor mode, this pin becomes $\overline{RD}$. When the MCU is in EPROM program mode, the pin is used as $\overline{OE}$ (EPROM memory output enable).	33
$P4_0$/$\overline{EDMA}$	I/O	CMOS I/O port ($\overline{EDMA}$: Expanded Data Memory Access). When the MCU is in memory expansion or microprocessor mode, this pin can become the $\overline{EDMA}$ pin.	24
$P4_1$/INT0 ~ $P4_2$/INT1	I/O	CMOS I/O port or external interrupt ports INT0 and INT1. These external interrupts can be configured to be active high or low.	23-22
$P4_3$/CNTR0	I/O	CMOS I/O port or Timer X input pin for pulse width measurement mode and event counter mode or Timer X output pin for pulse output mode. This pin can also be used as an external interrupt when Timer X is not in output mode. The interrupt polarity is selected in the Timer X mode register.	21
$P4_4$/CNTR1	I/O	CMOS I/O port or Timer Y input pin for pulse period measurement mode, pulse H-L measurement mode and event counter mode or Timer Y output pin for pulse output mode. This pin can also be used as an external interrupt when Timer Y is not in output mode. The interrupt polarity is selected in the Timer Y mode register.	20
$P5_0$/XC_{in}	I/O	CMOS I/O port or XC_{in}.	12
$P5_1$/T_{out}/ XC_{out}	I/O	CMOS I/O port or Timer 1/2 pulse output pin (can be configured initially high or initially low), or XC_{out}.	11
$P5_2$/OBF_0	I/O	CMOS I/O port or OBF_0 output to master CPU for data bus buffer 0.	8
$P5_3$/$\overline{IBF}_0$	I/O	CMOS I/O port or $\overline{IBF}_0$ output to master CPU for data bus buffer 0.	7
$P5_4$/$\overline{S}_0$	I/O	CMOS I/O port or $\overline{S}_0$ input from master CPU for data bus buffer 0.	6
$P5_5$/A_0	I/O	CMOS I/O port or A_0 input from master CPU.	5
$P5_6$/$\overline{R}$(E)	I/O	CMOS I/O port or $\overline{R}$(E) input from master CPU.	4
$P5_7$/$\overline{W}$(R/$\overline{W}$)	I/O	CMOS I/O port or $\overline{W}$(R/$\overline{W}$) input from master CPU.	3
$P6_0$/DQ0 ~ $P6_7$/DQ7	I/O	CMOS I/O port or master CPU data bus.	2-1, 80-75
USB D^-	I/O	USB D- voltage line interface, a series resistor of 33 Ω should be connected to this pin. (see note)	71
USB D^+	I/O	USB D+ voltage line interface, a series resistor of 33 Ω should be connected to this pin. (see note)	70
$P7_0$/$\overline{SOF}$	I/O	CMOS I/O port or USB start of frame pulse output, an 80 ns pulse outputs on this pin for every USB frame.	69
$P7_1$/$\overline{HOLD}$	I/O	CMOS I/O port or $\overline{HOLD}$ pin.	68
$P7_2$/$\overline{S}_1$	I/O	CMOS I/O port or $\overline{S}_1$ input from master CPU for data bus buffer 1.	67

Name	I/O	Description	Pin #
$P7_3/\overline{IBF_1}/\overline{HLDA}$	I/O	CMOS I/O port or $\overline{IBF_1}$ output to master CPU for data bus buffer 1, or $\overline{HLDA}$ pin. $\overline{IBF_1}$ and $\overline{HLDA}$ are mutually exclusive. $\overline{IBF_1}$ has priority over $\overline{HLDA}$.	66
$P7_4/OBF_1$	I/O	CMOS I/O port or OBF_1 output to master CPU for data bus buffer 1.	65
$P8_0$/UTXD2/$\overline{SRDY}$	I/O	CMOS I/O port or UART2 pin UTXD2 or SIO pin $\overline{SRDY}$. UART2 and SIO are mutually exclusive, UART2 has priority over SIO.	32
$P8_1$/URXD2/SCLK	I/O	CMOS I/O port or UART2 pin URXD2 or SIO pin SCLK. UART2 and SIO are mutually exclusive, UART2 has priority over SIO.	31
$P8_2/\overline{CTS2}$/SRXD	I/O	CMOS I/O port or UART2 pin $\overline{CTS2}$ or SIO pin SRXD. UART2 and SIO are mutually exclusive, UART2 has priority over SIO.	30
$P8_3/\overline{RTS2}$/STXD	I/O	CMOS I/O port or UART2 pin $\overline{RTS2}$ or SIO pin STXD. UART2 and SIO are mutually exclusive, UART2 has priority over SIO.	29
$P8_4$/UTXD1	I/O	CMOS I/O port or UART1 pin UTXD1.	28
$P8_5$/URXD1	I/O	CMOS I/O port or UART1 pin URXD1.	27
$P8_6/\overline{CTS1}$	I/O	CMOS I/O port or UART1 pin $\overline{CTS1}$.	26
$P8_7/\overline{RTS1}$	I/O	CMOS I/O port or UART1 pin $\overline{RTS1}$.	25
AV_{cc},AV_{ss}	I	**Power supply inputs for analog circuitry AV_{cc} = 4.15V ~ 5.25V or 3.00 ~ 3.6V, AV_{ss} = 0V**	17,19
CNV_{ss}	I	Controls the processor mode of the chip. Normally connected to V_{ss} or V_{cc}. When the MCU is in EPROM program mode, this pin supplies the programming voltage to the EPROM.	9
V_{cc},V_{ss}	I	**Power supply inputs: V_{cc} = 4.15 ~ 5.25V or 3.00 ~ 3.6V, V_{ss} = 0V**	16/74, 13/73
$\overline{RESET}$	I	To enter the reset state, this pin must be kept L for more that 2µs (20 Φ cycles under normal V_{cc} conditions). If the crystal or ceramic resonator requires more time to stabilize, extend this L level time appropriately.	10
XC_{in} XC_{out}	I O	An external ceramic or quartz crystal oscillator can be connected between the XC_{in} and XC_{out} pins. If an external clock source is used, connect the clock source to the XC_{in} pin and leave the XC_{out} pin open.	12 11
X_{in} X_{out}	I O	Input and output signals to and from the internal clock generation circuit. Connect a ceramic resonator or quartz crystal between X_{in} and X_{out} pins to set the oscillation frequency. If an external clock is used, connect the clock source to the X_{in} pin and leave the X_{out} pin open.	14 15
LPF	O	Loop filter for the frequency synthesizer.	18
Ext. Cap	I	An external capacitor (Ext. Cap) pin. When the USB transceiver voltage converter is used **in the Vcc = 5V application**, a 2µf or larger capacitor should connect between this pin and V_{ss} to ensure proper operation of the USB line driver. The voltage converter is enabled by setting bit 4 of the USB control register (0013_{16}) to a "1". **For Vcc = 3.3V applications, the Ext. Cap pin should be connected directly to Vcc in order to power the USB tranceiver.**	72

D+/D- Line driver notes: In order to match the USB cable impedance, a series resistor of 33Ω, 1%, 1/8 W should be connected to each USB line; i.e. on D+ (pin 70) and on D- (pin 71). Also, a coupling capacitor with the recommended value of 33pF should be connected between D+ and D- after the 33Ω series resistors. If the USB line is improperly terminated or not matched, signal fidelity will suffer, resulting in excessive overshoot or undershoot. This will potentially introduce bit errors.

VDD/VSS notes: In order to reduce the effects of the inductance of the traces on the board, decoupling capacitors should be connected between pins 73(VSS) and 74(VDD), 13(VSS) and 16(VDD), and 17(AVDD) and 19(AVSS). Recommended values are a 4.7 µF in parallel with a 0.1 µF.

VDD/VSS decoupling capacitor connections

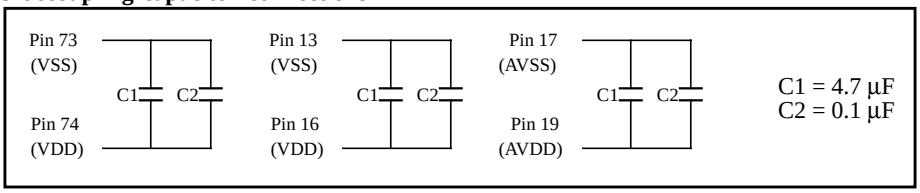


Figure 0-2.

The 7600 series, an enhanced family of CMOS 8-bit microcontrollers, offers high-speed operation at low voltage, large internal-memory options, and a wide variety of standard peripherals. The series is code compatible with the M38000, M37200, M37400, and the M37500 series, and provides many performance enhancements to the instruction set.

This device is a single chip PC peripheral microcontroller based on the Universal Serial Bus (USB) Version 1.0 specification. This device provides data exchange between a USB-equipped host computer and PC peripherals such as telephones, audio systems and digital cameras. See Figure 1-1 for an application system diagram.

The USB function control unit can support all four data transfer types listed in the USB specification: Control, Isochronous, Interrupt, and Bulk. Each transfer type is used for controlling a different set of PC peripherals. Isochronous transfers provide guaranteed bus access, a constant data rate, and error tolerance for devices such as computer-telephone integration (CTI) and audio systems. Interrupt transfers are designed to support human input devices (HID) that communicate small amounts of data infrequently. Bulk transfers are necessary for devices such as digital cameras and scanners that communicate large amounts of data to the PC as bus bandwidth becomes free. Finally, control transfers are supported and are useful for bursty, host-initiated type communication where bus management is the primary concern.